CLAIMS:

What is claimed is:

1. A method in a data processing system for providing hardware assistance to prefetch data during execution of code by a process or in the data processing system, the method comprising:

responsive to loading of an instruction in the code into a cache, determining, by a processor unit, whether metadata for a prefetch is present for the instruction; and

responsive to metadata being present for the instruction, selectively prefetching data, from within a data structure using the metadata, into the cache in a processor.

2. The method of claim 1, wherein the selectively prefetching step comprises:

determining whether outstanding cache misses are present; and

prefetching the data if a number of outstanding cache misses are less than a threshold.

3. The method of claim 1, wherein the selectively prefetching step includes:

determining whether to replace cache lines; and

prefetching the data if a number of cache lines chosen to be replaced are greater than a threshold.

4. The method of claim 1, wherein the selectively prefetching step includes:

retrieving the data from within the data structure using a pointer and an offset value.

5. The method of claim 1, wherein the selectively prefetching step includes:

retrieving the data from the data structure using an address.

6. The method of claim 1, wherein the processor unit is selected from one of an instruction cache or a load/store unit.

7. The method of claim 1, wherein the cache is an instruction cache.

8. The method of claim 4, wherein the metadata includes the pointer and the offset value.

9. A data processing system comprising:

a cache in a processor in the data processing system; and

a load/store unit in the processor, wherein the load/store unit determines whether metadata for a prefetch is present in response to loading an instruction for execution into a cache, the load/store unit selectively prefetches data from within a data structure into the cache using the metadata associated with the instruction.

10. The data processing system of claim 9, wherein the metadata is an address to the data within the data structure.

11. The data processing system of claim 9, wherein the metadata is a pointer and an offset to the data within the data structure.

12. A data processing system for providing hardware assistance to prefetch data during execution of code by a process or in the data processing system, the data processing system comprising:

determining means, responsive to loading of an instruction in the code into a cache, for determining, by a processor unit, whether metadata for a prefetch is present for the instruction; and

selectively prefetching means, responsive to metadata being present for the instruction, for selectively prefetching data, from within a data structure using the metadata, into the cache in a processor.

13. The data processing system of claim 12, wherein the selectively prefetching means comprises:

first means for determining whether outstanding cache misses are present; and

second means for prefetching the data if a number of outstanding cache misses are less than a threshold.

14. The data processing system of claim 12, wherein the selectively prefetching means includes:

first means for determining whether to replace cache lines; and

second means for prefetching the data if a number of cache lines chosen to be replaced are greater than a threshold.

15. The data processing system of claim 12, wherein the selectively prefetching means includes:

retrieving means for retrieving the data from within the data structure using a pointer and an offset value.

16. The data processing system of claim 12, wherein the selectively prefetching means includes:

retrieving means for retrieving the data from the data structure using an address.

17. The data processing system of claim 12, wherein the processor unit is selected from one of an instruction cache or a load/store unit.

18. A computer program product in a computer readable medium for providing hardware assistance to prefetch data during execution of code by a process or in the data processing system, the computer program product comprising:

first instructions, responsive to loading of an instruction in the code into a cache, for determining, by

a processor unit, whether metadata for a prefetch is present for the instruction; and

second instructions, responsive to metadata being present for the instruction, for selectively prefetching data, from within a data structure using the metadata, into the cache in a processor.

19. The computer program product of claim 18, wherein the second instructions comprises:

first sub-instructions for determining whether outstanding cache misses are present; and

second sub-instructions for prefetching the data if a number of outstanding cache misses are less than a threshold.

20. The computer program product of claim 18, wherein the second instructions includes:

first sub-instructions for determining whether to replace cache lines; and

second sub-instructions for prefetching the data if a number of cache lines chosen to be replaced are greater than a threshold.

21. The computer program product of claim 18, wherein the second instructions includes:

sub-instructions for retrieving the data from within the data structure using a pointer and an offset value.

22. The computer program product of claim 18, wherein the second instructions includes:

sub-instructions for retrieving the data from the data structure using an address.

23. The computer program product of claim 18, wherein the processor unit is selected from one of an instruction cache or a load/store unit.